R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

SUPPORT FOR THE CLAIM AMENDMENTS

Support for the claim amendments may be found in claim 3 (moved into claim 1) and claim 22 (moved into claim 20). Thus, no new matter has been added.

TELEPHONE INTERVIEW SUMMARY

Applicant's representative, John Ignatowski, spoke with Examiner Adam and Supervisor Zimmerman on May 5th regarding how the Examiner was applying the references to the claims. Claims 1, 15, 7, 16 and 23 were discussed in detail. To answer a question posed during the discussion, the application generally describes a system bus 16 in the specification on page 2, lines 1-4 and FIG. 2. The system bus 16 provides bi-directional communications between a graphics CPU 12, a memory 14 and a pixel pipeline circuit 20. No agreement was reached regarding the merits of the claims.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 1, 3-7, 20-22 and 30 under 35 U.S.C. §103(a) as being unpatentable over Murphy '919 in view of Chamberlin '785 is respectfully traversed and should be withdrawn.

The rejection of claims 8-10 and 23-24 under 35 U.S.C. §103(a) as being unpatentable over Murphy and Chamberlin in view of Chiu '391 is respectfully traversed and should be withdrawn.

The rejection of claims 11, 13, 14, 25 and 26 under 35 U.S.C. §103(a) as being unpatentable over Murphy and Chamberlin in view of Prouty '658 is respectfully traversed and should be withdrawn.

The rejection of claims 15-19 and 27-29 under 35 U.S.C. §103(a) as being unpatentable over Murphy and Chamberlin in view of Ozcelik, Patent Publication No. 2002/0149626 has been obviated by appropriate amendment and should be withdrawn.

Murphy concerns a graphics system with optimized use of unified local and frame buffers (Title). Chamberlin concerns a microprocessor having instruction fetch and execution overlap (Title). Chiu concerns a scaleable refresh display controller (Title). Prouty concerns a method and apparatus for raster computer graphic display of rotation invariant line styles (Title). Ozcelik concerns a display unit architecture (Title).

Claim 1 provides (i) a bus having a first address range and a second address range and (ii) a plurality of registers within the first address range. Page 2 of the Office Action asserts that (i) the GLINT register file of Murphy is similar to the claimed plurality of registers and (ii) FIG. 5C of Murphy illustrates a bus similar to the claimed bus. Per column 13, lines 8-12 of Murphy,

the register file appears as part of Region 0 of a PCI address map. The Host Bus in FIG. 5C of Murphy appears to be the only element capable of being a PCI bus. Therefore, the Office action appears to assert that the Host Bus of Murphy is similar to the claimed bus.

Claim 1 also provides a control circuit configured to control writing of data in a memory across the bus by driving an address onto the bus. During the telephone interview, the Examiner identified a Routing and control block in FIG. 5D of Murphy as being similar to the claimed control circuit. However, the Routing and control block in FIG. 5D of Murphy is shown in FIG. 5C (labeled Memory Interface) as having a direct connection to a DRAM and VRAM. Therefore, Murphy appears to be silent regarding a control circuit writing data in a memory across **the** bus. Chamberlin does not appear to cure the deficiency of Murphy. As such, Murphy and Chamberlin, alone or in combination, do not teach or suggest a control circuit configured to control writing of data in a memory across the bus by driving an address onto the bus as presently claimed.

Claim 1 further provides a memory directly connected to a bus for storing data corresponding to a pixel. Page 2 of the Office Action admits that Murphy does not explicitly disclose a memory directly connected to a bus and responsive within a second range. The Office Action asserts that Chamberlin cures the above

deficiency by disclosing a memory (ROM 83) directly connected to a bus 79. However, FIG. 1 of Chamberlin shows that the ROM 83 is **indirectly** coupled to the address bus 79 with a SEL 81 circuit between. Chamberlin does not appear to teach or suggest a memory directly connected to a bus as asserted in the Office Action. Therefore, Murphy and Chamberlin, alone or in combination, do not teach or suggest a memory directly connected to a bus for storing data corresponding to a pixel as presently claimed.

Claim 1 further provides (from claim 3) a clipping circuit configured to generate a clipping signal. In contrast, Murphy appears to be silent regarding a clipping function of the GLINT graphics processor generating a signal. Furthermore, the Office Action provides no evidence or argument where Murphy indicates generating a clipping signal. Therefore, Murphy and Chamberlin, alone or in combination, do not teach or suggest a clipping circuit configured to generate a clipping signal as presently claimed.

Furthermore, the Office Action fails to provide particular findings as to the reasons a skilled artisan, with no knowledge of the presently claimed invention, would have selected the cited references for combination. The factual inquiry whether to combine references must be thorough and searching. The rigorous application of the requirement for showing the teaching or motivation to combine references is necessary to avoid the subtle

but powerful attraction of a hindsight-based obviousness analysis. It is improper, in determining whether a person of ordinary skill in the art would have been led to the combination of references, simply to use that which the inventor taught against its teacher.

No motivation appears to exist for one of ordinary skill in the art to move the DRAM and/or VRAM memory from the dedicated interface to the Memory Interface shown in FIG. 5C of Murphy to the PCI host bus. The fact that references can be combined or modified is not sufficient to establish *prima facie* obviousness (MPEP §2143.01). Furthermore, moving the DRAM and VRAM memory from a dedicated interface to a general purpose bus, such as PCI, would appear to slow down an access speed to the memory, not increase the speed as asserted on page 3 of the Office Action. Still further, the Office Action fails to provide evidence of a reasonable expectation of success to move the memory to the host bus. Because the Office Action fails to provide particular findings as to the reasons a skilled artisan, with no knowledge of the presently claimed invention, would have selected the cited references for combination, the Office Action does not appear to have met the Office's burden of factually establishing a *prima facie* case of obviousness (MPEP §2142). Claims 15, 20 and 30 provide language similar to the above argued portions of claim 1. As such, the claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Regarding claim 15, the Office Action fails to establish *prima facie* obviousness to combine Murphy and Chamberlin with Ozcelik. Page 8 of the Office Action asserts that motivation to combine is to "increase flexibility in defining displays." The text of Ozcelik cited by the Office Action reads:

> Thus, there is a need for a display hardware that has a relatively low hardware complexity yet provides substantial flexibility in defining displays.

However, no explanation or evidence is provided by the Office Action why the substantial flexibility of Ozcelik is an increase as compared with the proposed combination of Murphy and Chamberlin. Therefore, the asserted motivation appears to be a conclusory statement lacking supporting evidence so *prima facie* obviousness has not been established. As such, claim 15 is fully patentable over the cited references and the rejection should be withdrawn.

Claim 20 further provides steps for (i) memory mapping a first register storing an X coordinate to a first location and a second location in a first address range and (ii) memory mapping a second register storing a Y coordinate to a third location and a fourth location in the first address range. Despite the assertion on page 4 of the Office Action, the text in column 13, lines 13-18 and 26-28 of Murphy appear to be silent regarding a register memory mapper to two locations. The text of Murphy cited by the Office Action states:

> When a GLINT host software driver is initialized it can map the register file into its address space. Each register has

> an associated address tag, giving its offset from the base of the register file (since all registers reside on a 64-bit boundary, the tag offset is measured in multiples of 8 bytes).
> ...
> The last write triggers the start of rendering. GLINT has approximately 200 registers.

Nowhere in the above text, or in any other section, does Murphy appear to discuss a register memory mapped to two locations. Therefore, Murphy and Chamberlin, alone or in combination, do not teach or suggest steps for (i) memory mapping a first register storing an X coordinate to a first location and a second location in a first address range and (ii) memory mapping a second register storing a Y coordinate to a third location and a fourth location in the first address range as presently claimed.

The interpretation provided during the telephone interview that Murphy provides addressing to individual bytes within a single register file does not appear to match the language of Murphy. In particular, column 13, lines 15-23 of Murphy state:

> Each register has an associated address tag, giving its offset from the base of the register file (since all registers reside on a 64-bit boundary, **the tag offset is measured in multiples of 8 bytes**). The most straightforward way to load a value into a register is to write the data to its mapped address. In reality the chip interface comprises a 16 entry deep FIFO, and **each write to a register causes the written value and the register's address tag to be written as a new entry in the FIFO.** (Emphasis added)

Accessing a register involves passing the address tag thru the FIFO but the PCI address appears to stop at the FIFO. A single tag offset step appears to represent a 64-bit (8 bytes) step in the

register file. Since each register is 64 bits wide, the address tag only appears to be capable of addressing whole registers at a time. Therefore, Murphy and Chamberlin, alone or in combination, do not teach or suggest steps for mapping registers to multiple locations as presently claimed. As such, claim 20 is fully patentable over the cited references and the rejection should be withdrawn.

Claim 4 provides a control circuit configured to inhibit writing of data to an address in response to a clipping signal. Page 3 of the Office Action admits that Murphy does not teach inhibiting writing. Instead, the Office Action asserts that it is inherent not to process extraneous data. Applicants' representative respectfully traverses the assertion of inherency to not process extraneous data. In particular, column 8, lines 44-48 of Murphy state:

> When the Depth Block receives a message "new fragment", it will calculate the corresponding depth and do the depth test. If the test passes then the "new fragment" message is passed to the next unit. **If the test fails then the message is modified and passed on.** (Emphasis added)

Since inherency requires certainty of results, not mere possibility, the functionality of Murphy to continue to pass fragments failing the depth test indicates that not processing extraneous data is not a certainty and thus cannot be inherent. Therefore, *prima facie* obviousness to modify Murphy to not write clipped pixel data has not been established. Claim 21 provides

language similar to claim 4. As such, the Examiner is respectfully requested to either (i) provide clear and concise evidence why having values outside a clipping window necessarily results in inhibiting writing of those values or (ii) withdraw the rejection.

Claim 8 provides an address decoder for (i) monitoring a first, a second, a third and a fourth memory locations and (ii) applying a location signal to a control circuit representative of an address location being written to. In contrast, Murphy, Chamberlin and Chiu each appear to be silent regarding a circuit that both monitors multiple locations and generated a signal representative of which of the multiple locations is being written to. Furthermore, a control signal associated with the address decoder 206 of Chiu appears to be an input received by the address decoder 206, not an output signal generated by the address decoder 206. Therefore, Murphy, Chamberlin and Chiu, alone or in combination, do not appear to teach or suggest an address decoder for (i) monitoring a first, a second, a third and a fourth memory locations and (ii) applying a location signal to a control circuit representative of an address location being written to as presently claimed.

Furthermore, the Office Action does not provide any evidence of motivation from either the references or knowledge generally available to one of ordinary skill in the art to modify or combine as required by MPEP §2142. In particular, the text on

page 5, lines 1-5 of the Office Action makes no mention of Murphy, Chamberlin, Chiu or generally available knowledge. Therefore, *prima facie* obviousness has not been established. Claim 23 provides language similar to claim 8. As such, claims 8 and 23 are fully patentable over the cited references and the rejection should be withdrawn.

Claim 14 provides an address decoder. In contrast, each of Murphy, Chamberlin and Prouty appear to be silent regarding an address decoder. Furthermore, the Office Action merely points to claim 8 in rejecting claim 14. However, the rejection of claim 8 relies on Chiu to teach an address decoder yet Chiu is not part of the basis for rejecting claim 14. Therefore, Murphy, Chamberlin and Prouty, alone or in combination, do not appear to teach or suggest an address decoder as presently claimed. As such, the Examiner is respectfully requested to either (i) provide evidence and a clear and concise explanation where at least one of Murphy, Chamberlin or Prouty teach or suggest an address decoder or (ii) withdraw the rejection.

Claim 16 provides a second register and a logic unit for writing data to the second register. In contrast, each of Chamberlin and Ozcelik appear to be silent regarding a logic unit writing data to a register. Furthermore, the multiplexer in FIG. 2B of Murphy does not appear to write to a register. Still further, FIG. 2B of Murphy appears to be silent regarding the

multiplexer writing in dependence on an address calculated by the graphics hyperpipline block (asserted similar to the claimed calculation circuit). The multiplexer in FIG. 2B of Murphy does not appear to be able to combine data for at least two pixels for storage in a single memory word. Furthermore, the fact that a multiplexer may time multiplex two parallel data items into two sequential data items is irrelevant to the claim which is silent regarding time multiplexing. Therefore, Murphy and Ozcelik, alone or in combination, do not teach or suggest a second register and a logic unit for writing data to the second register as presently claimed. As such, claim 16 is fully patentable over the cited references and the rejection should be withdrawn.

Claim 19 provides that the control circuit is further configured to combine data for pixels in response to a receipt of the same address signal. In contrast, each of Murphy, Chamberlin and Ozcelik appear to be silent regarding a control circuit combining pixel data upon receipt of an address signal. Furthermore, the assertion on page 8 of the Office Action that "the remarks directed to claims 1 and 18, above, apply equally to this claim" makes no sense. Nothing in the rejections of claims 1 and 18 discussed combining data for pixels. Therefore, Murphy and Ozcelik, alone or in combination, do not appear to teach or suggest a control circuit configured to combine data for pixels in response to a receipt of a same address signal as presently claimed. Claim

28 provides language similar to claim 19. As such, claims 19 and 28 are fully patentable over the cited reference and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

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